

A diagram of a cell, labeled 'D' and 'T'. It shows a large outer oval boundary and a smaller inner oval boundary, both with dashed lines. The space between the boundaries is labeled 'D', and the space inside the inner boundary is labeled 'T'.

FIG. 1B

A2

A1

A3

G

L

G

L

G

L

M

G

1

2

1

2

Lb

La

Tg

Tc

Pd

L

L1

L2

L1

L2

Tb

Ta

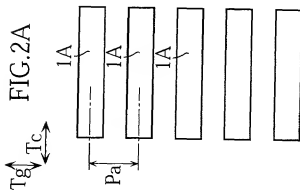


FIG. 2B

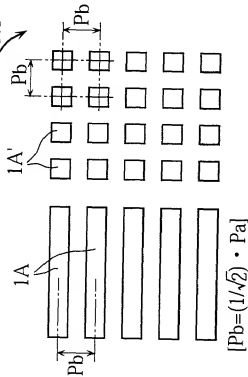


FIG. 2C

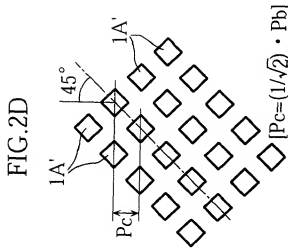


FIG. 2E

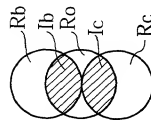


FIG. 2F

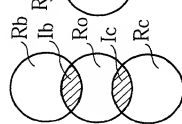


FIG. 2G

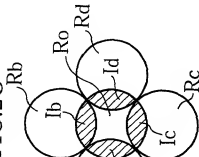


FIG. 2H

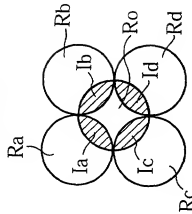


FIG.3A

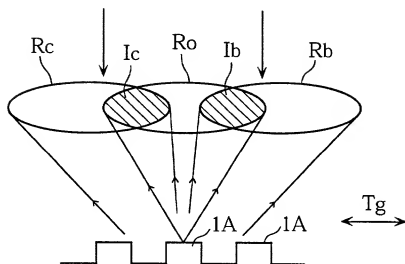


FIG.3B

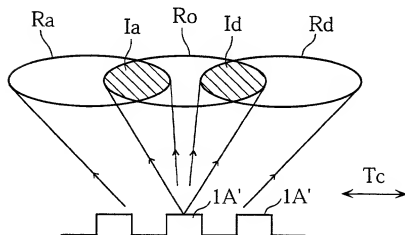


FIG.4

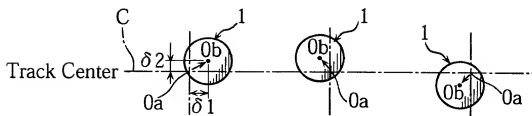
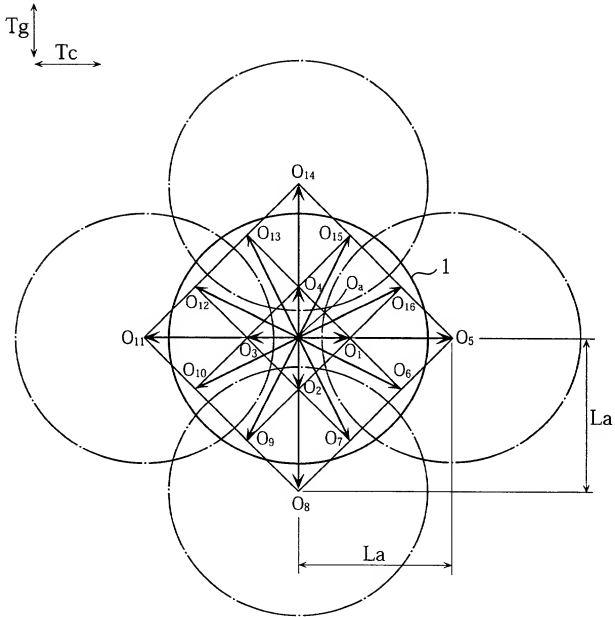


FIG.5



The diagram illustrates a sector of a disk with concentric tracks and radial sectors. The tracks are labeled A1, A2(1), A2(2), A2(3), A2(n-1), A2(n), and A3. The sectors are labeled A1, A2, A3, and A3. The diagram shows the layout of data on the disk, including a reference data area and a recording area. The timing parameters T_c and T_g are indicated. The diagram also shows the layout of data on the disk, including a reference data area and a recording area.

FIG. 7

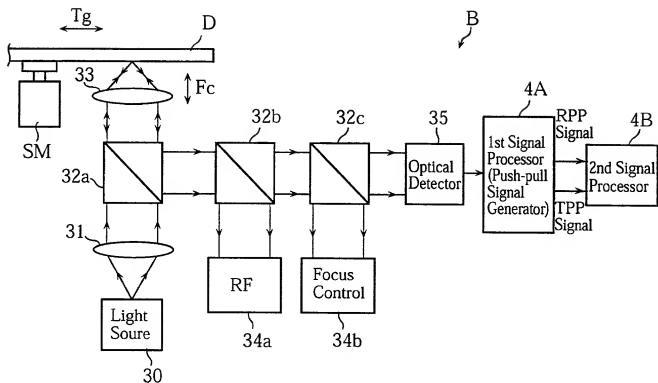
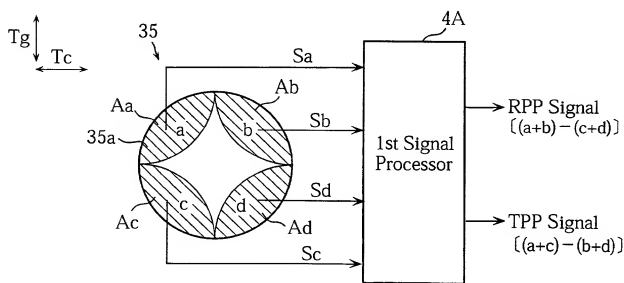


FIG. 8



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FIG.9A

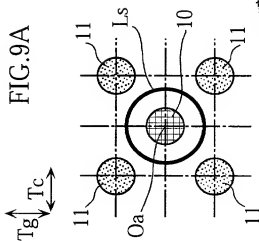


FIG.9B

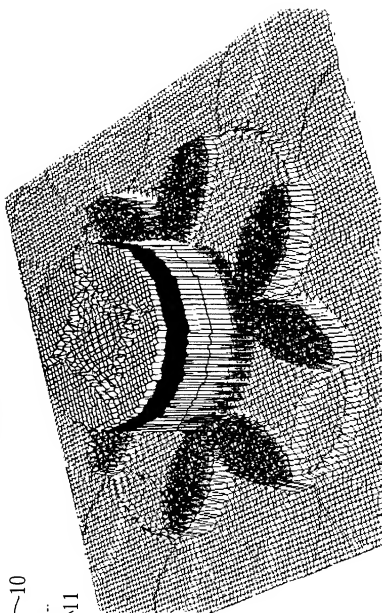


FIG.10A

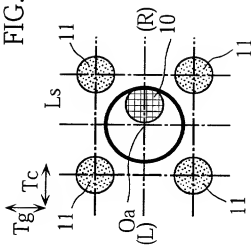


FIG.10B

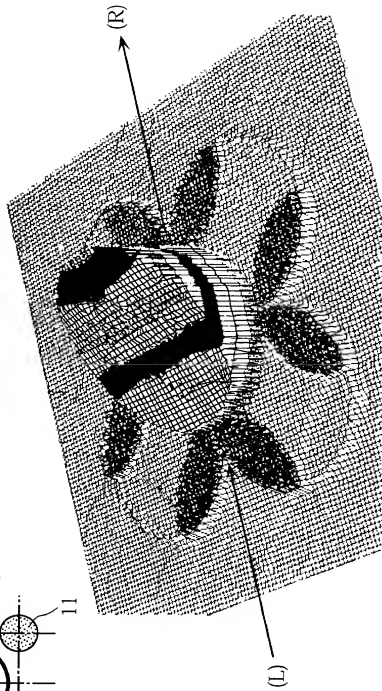


FIG.11A

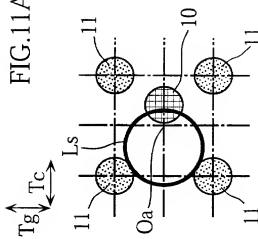
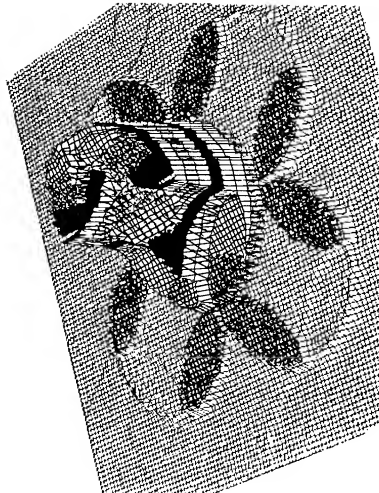


FIG.11B



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FIG.12A

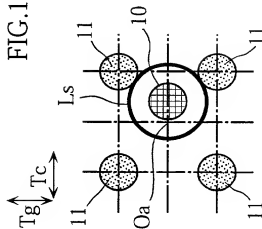


FIG.12B

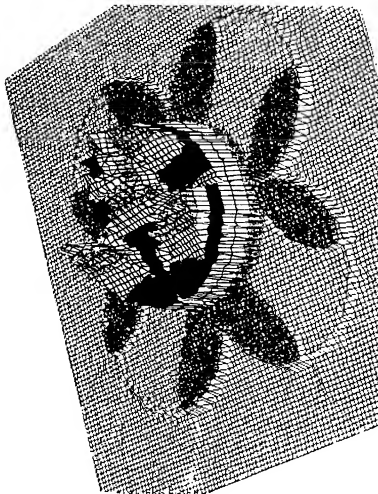


FIG.13A

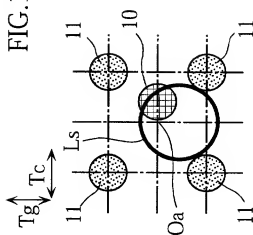
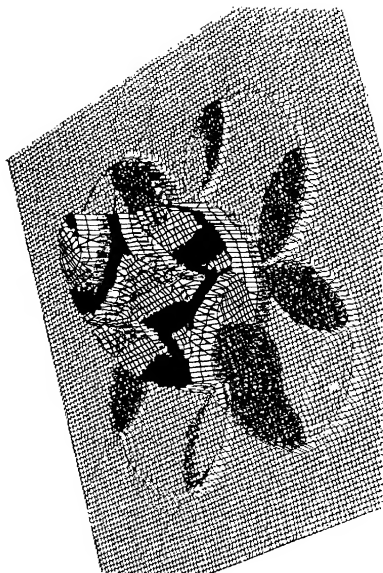


FIG.13B



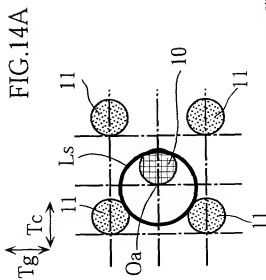


FIG.14B

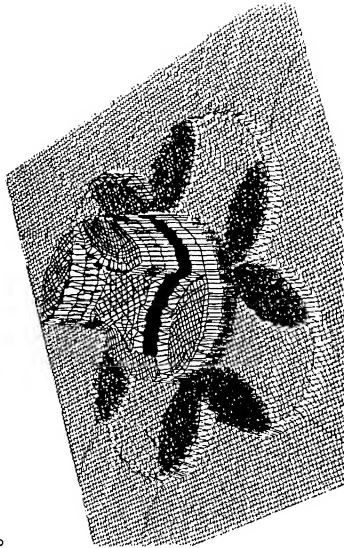


Figure 1 is a block diagram of a tracking error signal processing circuit. The circuit takes two input signals, TPP Signal and RPP Signal, and a Read/Write Channel Clock. The TPP Signal is converted to digital by A/D converter 41, then processed by PLL 42. The RPP Signal is sampled by S/H 40a and 40b. The PLL output is filtered by 47 and then sampled by 40a and 40b. The outputs of 40a and 40b are processed by comparators 43a and 43b, which also receive feedback signals V1, V2, and V3. The outputs of 43a and 43b are processed by CMP blocks 44a and 44b, then decoders 45a and 45b, and finally latches 46a and 46b to produce Data XX and Data YY. A truth table for TPP+RPP is provided at the bottom.

TPP+RPP	V1	V2	V3
XX	001	001	001
	010	010	010
	101	101	101
	111	111	111

FIG.16B

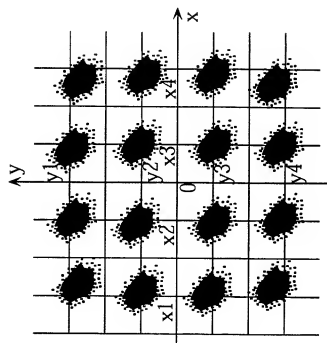


FIG.16A

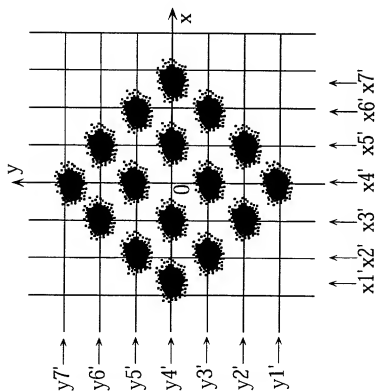


FIG.17

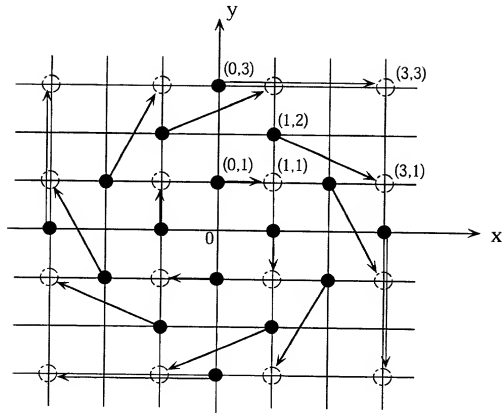


FIG.18

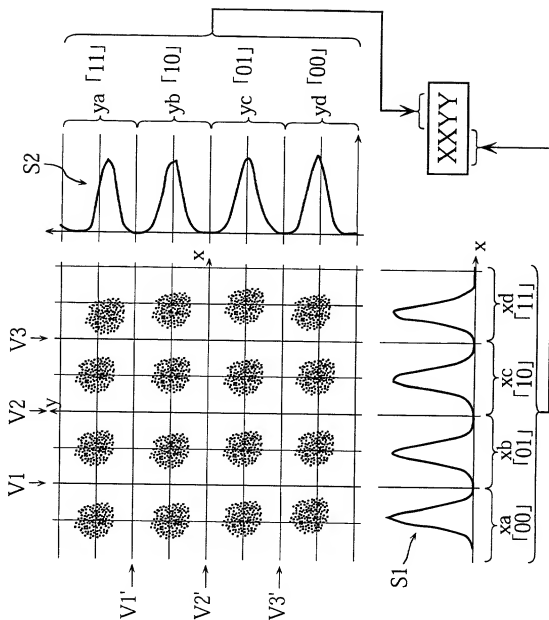


FIG. 19

The diagram illustrates a superconducting junction device and its temperature dependence of resistance. The top part is a schematic of the device structure, showing a central region (A2) with layers of Pt, Na, and Nb, and two outer regions (A1 and G2) with layers of Pt and Nb. The thicknesses of the Pt and Na layers are labeled L and G, respectively. The temperature dependence of the resistance is shown in the bottom part, with four curves labeled (a) through (d). The x-axis represents temperature T, with T_g and T_c marked. The y-axis represents resistance R. The curves show a sharp increase in resistance at T_c and a sharp decrease at T_g. The curves are labeled: (a) TPP Signal(Ta), (b) TPP Signal(Tb), (c) RPP Signal(Ta), and (d) RPP Signal(Tb).

FIG. 20
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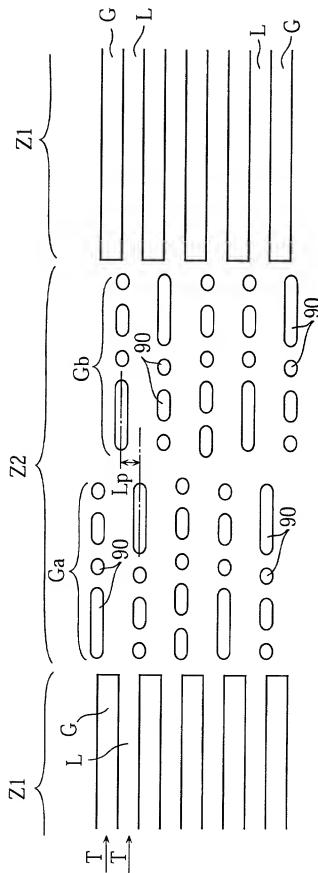


FIG.21
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